

## CLAIMS

1-9. (Cancelled)

10. (Currently Amended) A bias tuning circuit for a MRAM comprising, in combination:

- a bias generator having a bias output;
- a plurality of switches, each of the switches having a word reference input and a mirror transistor output;
- a plurality of mirror transistors connected to ~~one of~~ the mirror transistor outputs;
- a transistor connected to the bias output of the bias generator and further connected in a mirror configuration with the plurality of mirror transistors and having a tuned reference output;

and

a selector to select one of the mirror ~~transistors~~ transistor to activate the transistor to set ~~[[the]]~~ a voltage to the plurality of mirror transistors.

11. (Original) The bias tuning circuit of claim 10 with the each one of the plurality of mirror transistors having a different gain.

12. (Currently Amended) The bias tuning circuit of claim 10 further comprising, in combination:

- a pad;
- a indicator transistor in a mirror configuration with the transistor and connected to the pad to provide an indicator.

13. (Original) The bias tuning circuit of claim 12 with the pad being an external pad.

14. (Original) The bias tuning circuit of claim 12 with the indicator transistor having a gain that is a multiple of the transistor.
15. (Original) The bias tuning circuit of claim 10 with the plurality of mirror transistors are n-channel transistors.
16. (Original) The bias tuning circuit of claim 10 with the plurality of switches being transistors.
17. (Original) The bias tuning circuit of claim 10 with the transistor being an N-channel transistor.
18. (Original) The bias tuning circuit of claim 10 with the bias generator being a temperature and voltage compensated bias generator.
19. (Currently Amended) The bias tuning circuit of claim 10 with the selector selecting one of the plurality of mirror transistors to ~~compensate~~ compensate for a tested parameter.
20. (Currently Amended) The bias tuning circuit of claim ~~[[10]]~~ 19 with the tested parameter being a manufacturing variance.